UWB Baseband Processor

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Dept. of Electronics Engineering
NCTU
Outline

✓ Introduction
✓ Industry UWB Technology
✓ UWB Solutions in NCTU
✓ Conclusion
Introduction - Wireless Access Trend

Wireless Access Trend

- **Bandwidth**
  - 1 Gbps
  - 100 Mbps
  - 10 Mbps
  - 1 Mbps

- **Distance**
  - < 1m: Desktop
  - 10 m: Room
  - 100 m: Building
  - > 1 Km: Community

- **WPAN**
  - Future Generations UWB
  - UWB-based technology launches at 500Mbps
  - Roadmap generations up to 1Gbps

- **WLAN**
  - Next generation 802.11
  - 802.11a
  - 802.11b/ g

- **WWAN**
  - 3G
  - 2.5G
  - 3+G

The way where we’re.
Introduction - Motivation

✓ Drive system design methodology
  - System performance
  - Reduce power consumption
  - Link to CMOS processes

✓ Essential IP’s
  - Uniqueness
  - Reuse
  - Participation in Standard Draft
Block diagrams of 11a/g PHY system
In general synchronization design, more than 80% of preamble is used.

We propose a low-complexity synchronization using 37.5% preamble and reduce 42.5% synchronization complexity.

Average 0.2~0.3dB SNR loss is traded.

Frame detection

Automatic frequency control

Proposal

Data rate: 54Mbits/s
Introduction - SNR-controlled

- Decision-directed tracking-based channel estimation (CE) is generally applied for high system performance.
- We propose a feedback CE with Computation-save control (CSC) to reduce CE-tracking complexity.
- Average 0.3dB SNR loss is traded.

Data rate: 54Mbits/s

Proposal

Turned off by CSC
PER simulation of the proposal

- The proposed low-complexity system has average 0.56 dB SNR loss than our previous system.

<table>
<thead>
<tr>
<th>Data rate (Mbits/s)</th>
<th>The proposed design SNR (dB)</th>
<th>Previous version design SNR (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>4.3</td>
<td>3.1</td>
</tr>
<tr>
<td>9</td>
<td>5.8</td>
<td>5.2</td>
</tr>
<tr>
<td>12</td>
<td>6.5</td>
<td>6.3</td>
</tr>
<tr>
<td>18</td>
<td>9.5</td>
<td>8.8</td>
</tr>
<tr>
<td>24</td>
<td>12.0</td>
<td>11.4</td>
</tr>
<tr>
<td>36</td>
<td>15.6</td>
<td>15.2</td>
</tr>
<tr>
<td>48</td>
<td>19.3</td>
<td>19.1</td>
</tr>
<tr>
<td>54</td>
<td>21.4</td>
<td>20.8</td>
</tr>
</tbody>
</table>

Multipath RMS delay: 50 ns, CFO: 40 ppm, clock offset: 40 ppm
The proposed design improves 0.85 ~ 6.66dB SNR gain compared with current solutions and standard requirement.

### Required SNR for 10% PER

<table>
<thead>
<tr>
<th>Data rate (Mbps)</th>
<th>This work (dB)</th>
<th>Reference [1]</th>
<th>Reference [2]</th>
<th>Required SNR of IEEE 802.11a (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>2.8</td>
<td>5.4</td>
<td>4.9</td>
<td>9.7</td>
</tr>
<tr>
<td>9</td>
<td>3.9</td>
<td>5.8</td>
<td>5.8</td>
<td>10.7</td>
</tr>
<tr>
<td>12</td>
<td>5.6</td>
<td>7.0</td>
<td>8.6</td>
<td>12.7</td>
</tr>
<tr>
<td>18</td>
<td>8.05</td>
<td>9.5</td>
<td>9.9</td>
<td>14.7</td>
</tr>
<tr>
<td>24</td>
<td>11.2</td>
<td>11.3</td>
<td>12.4</td>
<td>17.7</td>
</tr>
<tr>
<td>36</td>
<td>15.0</td>
<td>14.9</td>
<td>15.9</td>
<td>21.7</td>
</tr>
<tr>
<td>48</td>
<td>19.45</td>
<td>18.6</td>
<td>20.3</td>
<td>25.7</td>
</tr>
<tr>
<td>54</td>
<td>20.3</td>
<td>20.6</td>
<td>21.7</td>
<td>26.7</td>
</tr>
<tr>
<td>Average Better SNR Gain (dB)</td>
<td>0.85</td>
<td>1.65</td>
<td>6.66</td>
<td></td>
</tr>
</tbody>
</table>

Simulation environment: AWGN channel, CFO: 40ppm, SCO: 40ppm
✓ Complexity measurement in one typical packet including 1000 data bytes:

- Reduce 34% ~ 42% complex multiplication
- Reduce 63% ~ 96% of complex division
- Reduce 17% memory read
- Reduce 3% ~ 10%
Complexity comparison in one typical packet

Complex multiplication: Reduce 9K ~ 52K
Memory read: Reduce 10K ~ 96K bytes

Complex division: Reduce 1K ~ 15K
Memory write: Reduce 2K ~ 44K bytes
What’s Ultra Wideband (UWB)?

- FCC announced 3.1 ~ 10.6GHz RF Band for UWB application
- UWB signal bandwidth: ≥500MHz
- Data rate: Typical 110M ~ 480Mb/s
- Main application: IEEE 802.15.3a Wireless Personal Area Network (WPAN)
- Transmission distance: ≤ 10 meters
Introduction

✓ Applications

Home Entertainment

Computing

Mobile Devices

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Introduction

Print from handheld

Images from camera to storage/network

Exchange your music & data

Stream presentation from laptop/PDA to projector

MP3 titles to music player

Stream DV or MPEG to display
Main technology

- Multi-Band OFDM (MB-OFDM)
  - Multi-Band OFDM Alliance (MBOA):
    - *Intel, TI, Staccato, Wisair, Alereon*....

- Direct Sequence-UWB (DS-UWB)
  - *Motorola, Freescale, ............*
UWB papers in IEEE Library

- IEEE 802.15.3a Standard Meeting
- Indoor UWB Channel Model: > 75 papers
- Pulse-based UWB Baseband: > 40 papers
- DS-CDMA UWB baseband: > 10 papers
- OFDM-based UWB baseband: > 5 papers

Years:
- '97
- '02
- 03"
- 04"
- 05"

National Chiao Tung University
Outline

✓ Introduction

✓ Industry UWB Technology
  – MB-OFDM
  – DS-UWB

✓ NCTU UWB Techniques

✓ Conclusions
MB-OFDM Technology

- 3 band (Mode 1) and 7 band (Mode 2) hopping
- Signal bandwidth: 528MHz
## MB-OFDM Technology

### System Requirement

<table>
<thead>
<tr>
<th></th>
<th>110M</th>
<th>200M</th>
<th>480M</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data rate (b/s)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Min. transmission distance</td>
<td>10m</td>
<td>4m</td>
<td>2m</td>
</tr>
<tr>
<td>Range (AWGN)</td>
<td>20.5m</td>
<td>14.1m</td>
<td>7.8m</td>
</tr>
<tr>
<td>ADC/ DAC Wordlength</td>
<td>≥4-bit</td>
<td>≥4-bit</td>
<td>≥5-bit</td>
</tr>
</tbody>
</table>
MB-OFDM Technology

✓ Signal format

- PLCP Preamble / Header
- Frame Payload
  Variable Length: 0 – 4095 bytes
- FCS
- Tail Bits
- Pad Bits

- Zero-padded
- FFT symbol (Data and pilots)
- Guard interval

- 53.3Mb/s ~ 480Mb/s
- 60.6ns
- 242.4ns
- 9.5ns
**Multi-band transmission**

- Time-Frequency-interleaved (TFI) method

![Diagram](image)

- **Synchronization**
- **Header**
- **Channel Estimation**
- **Payload**

- Band #9
- Band #8
- Band #7
- Band #6
- Band #3
- Band #2
- Band #1

- **14.0625 usec (Preamble + Header)**

- **Channel Estimation Upper 4 Bands**
  - **Header on Lower 3 Bands**
  - **Payload**

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Advantages of multi-band design

- Lower ADC rate
- Against interference from U-NII

Power vs. Frequency

- Band #1: 1584 MHz
- Band #2: 528 MHz
- SIR < -8 dB
## Data Rate Parameter

<table>
<thead>
<tr>
<th>Data Rate (Mb/s)</th>
<th>53.3</th>
<th>80</th>
<th>110</th>
<th>160</th>
<th>200</th>
<th>320</th>
<th>480</th>
</tr>
</thead>
<tbody>
<tr>
<td>Modulation/Constellation</td>
<td>OFDM/QPSK</td>
<td>OFDM/QPSK</td>
<td>OFDM/QPSK</td>
<td>OFDM/QPSK</td>
<td>OFDM/QPSK</td>
<td>OFDM/QPSK</td>
<td>OFDM/QPSK</td>
</tr>
<tr>
<td>Coding Rate</td>
<td>1/3</td>
<td>1/2</td>
<td>11/32</td>
<td>1/2</td>
<td>5/8</td>
<td>1/2</td>
<td>3/4</td>
</tr>
<tr>
<td>Time-domain spreading</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Freq.-domain spreading</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
</tbody>
</table>
MB-OFDM Technology

✓ TX Architecture

General OFDM Blocks

Input Data → Scrambler → Convolutional Encoder → Puncturer → Bit Interleaver → Constellation Mapping → IFFT Insert Pilots Add Prefix/GI → DAC

exp(j2πf_d)

Spreading, Zero-padded

Time-Frequency Code
RX Architecture

General OFDM Blocks

Pre-Select Filter → LNA → LPF → AGC → Synchronization

VGA → Remove CP → FFT

ADC → Remove Pilots → De-Interleaver

Synchronization

Carrier Phase and Time Tracking

Viterbi Decoder → De-scrambler

Output Data

MB-controlling
Time-domain spreading: Save data from interference

No time-domain spreading: Data is distorted by interference

Time-domain spreading: Data is duplicated and saved.

Distorted by interference

Duplication
MB-OFDM Technology

✓ Frequency-domain spreading
  
  - Save the TX hardware power in imaginary part

\[ A^* \quad A \quad f \overset{\text{IFFT}}{\rightarrow} I \quad Q \]
Zero-padded (ZP): lower signal power than cyclic prefix (CP)
**Hardware power prediction of PHY (BB+RF+ADC)**

<table>
<thead>
<tr>
<th>Process</th>
<th>Rate (Mb/s)</th>
<th>TX</th>
<th>RX</th>
</tr>
</thead>
<tbody>
<tr>
<td>130nm</td>
<td>110</td>
<td>117mW</td>
<td>205mW</td>
</tr>
<tr>
<td></td>
<td>200</td>
<td>117mW</td>
<td>227mW</td>
</tr>
<tr>
<td></td>
<td>480</td>
<td>180mW</td>
<td>323mW</td>
</tr>
<tr>
<td>90nm</td>
<td>110</td>
<td>93mW</td>
<td>155mW</td>
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<tr>
<td></td>
<td>200</td>
<td>93mW</td>
<td>169mW</td>
</tr>
<tr>
<td></td>
<td>480</td>
<td>145mW</td>
<td>236mW</td>
</tr>
</tbody>
</table>
MB-OFDM Technology

✓ Industry Progress

Wisair: Evaluation Kit  RF Transceiver  480Mb/s BB-IC  Expected WUSB

Alereon, Staccato...

UWB Demo and products

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<table>
<thead>
<tr>
<th>Piconet Channel</th>
<th>Chip Rate</th>
<th>Center Frequency</th>
<th>Spreading Code Set</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1313 MHz</td>
<td>3939 MHz</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>1326 MHz</td>
<td>3978 MHz</td>
<td>2</td>
</tr>
<tr>
<td>3</td>
<td>1339 MHz</td>
<td>4017 MHz</td>
<td>3</td>
</tr>
<tr>
<td>4</td>
<td>1352 MHz</td>
<td>4056 MHz</td>
<td>4</td>
</tr>
<tr>
<td>5</td>
<td>1300 MHz</td>
<td>3900 MHz</td>
<td>5</td>
</tr>
<tr>
<td>6</td>
<td>1365 MHz</td>
<td>4094 MHz</td>
<td>6</td>
</tr>
<tr>
<td>7</td>
<td>2626 MHz</td>
<td>7878 MHz</td>
<td>1</td>
</tr>
<tr>
<td>8</td>
<td>2652 MHz</td>
<td>7956 MHz</td>
<td>2</td>
</tr>
<tr>
<td>9</td>
<td>2678 MHz</td>
<td>8034 MHz</td>
<td>3</td>
</tr>
<tr>
<td>10</td>
<td>2704 MHz</td>
<td>8112 MHz</td>
<td>4</td>
</tr>
<tr>
<td>11</td>
<td>2600 MHz</td>
<td>7800 MHz</td>
<td>5</td>
</tr>
<tr>
<td>12</td>
<td>2730 MHz</td>
<td>8190 MHz</td>
<td>6</td>
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</tbody>
</table>
### Rate Parameter

<table>
<thead>
<tr>
<th>Data Rate</th>
<th>FEC Rate</th>
<th>Code Length</th>
<th>Range (AWGN)</th>
</tr>
</thead>
<tbody>
<tr>
<td>28 Mbps</td>
<td>½</td>
<td>24</td>
<td>29 m</td>
</tr>
<tr>
<td>55 Mbps</td>
<td>½</td>
<td>12</td>
<td>23 m</td>
</tr>
<tr>
<td>110 Mbps</td>
<td>½</td>
<td>6</td>
<td>18.3 m</td>
</tr>
<tr>
<td>220 Mbps</td>
<td>½</td>
<td>3</td>
<td>13 m</td>
</tr>
<tr>
<td>500 Mbps</td>
<td>¾</td>
<td>2</td>
<td>7.3 m</td>
</tr>
<tr>
<td>660 Mbps</td>
<td>1</td>
<td>2</td>
<td>4.1 m</td>
</tr>
<tr>
<td>1000 Mbps</td>
<td>¾</td>
<td>1</td>
<td>5.1 m</td>
</tr>
<tr>
<td>1320 Mbps</td>
<td>1</td>
<td>1</td>
<td>2.9 m</td>
</tr>
</tbody>
</table>
TX Architecture

Input Data → Scrambler → K=6 FEC Encoder → Conv. Bit Interleaver → Bit-to-Code Mapping → Pulse Shaping → MBOK → $f_{LO}$
RX Architecture

- 1~3-bit ADC can be used

**Chip Rate ADC**

*Higher Performance some DSP-capable*

- Filter → Demod → ADC → Digital Correlator Bank → SAP
- 1.368 Gsps

**Symbol Rate ADC**

*Simple/cheap Analog Emphasis*

- Demod → Analog Correlator Bank → ADC → SAP
- 57 Msps
DS-UWB Technology

✓ DS-UWB Modulation

M-ary Bi-Orthogonal Keying

Data → ⊗ → Code

1 0 → 011100

100
DS-UWB Technology

DS-UWB power spectrum

TX Data

MBOK

TX Code

Channel

RX Data

De-MBOK

Gain

Interference

AWGN

National Chiao Tung University
Motorola/ Freescale Progress

- ’04 Q2: 110Mb/s RF-BB solution
- ’04 Q3: 110Mb/s UWB 1394 development
- ’04 Q4: 110Mb/s Mini-PCI development
- ’05 Q1: UWB mobile phone
Outline

- Introduction
- Industry UWB Technology
- NCTU UWB Techniques
  - 480Mb/s LDPC-COFDM
  - NCTU MB-OFDM
  - I/Q Mismatch
  - Dynamic sampling
  - 1GSps FFT Processor
  - 480Mb/s Viterbi-COFDM
  - 5Gb/s LDPC design
- Conclusions
NCTU Roadmap

- ’04 Q1-Q2: 480Mb/s LDPC-OFDM Chip Design
- ’04 Q3: 5Gb/s LDPC FEC Design
- ’04 Q4~’05 Q1: MB-OFDM Chip Design
- ’05 Q2: MB-OFDM BB/RF/MAC Integration
LDPC-OFDM Design Motivation

- OFDM modulation:
  High data rate of UWB and compatibility to WLAN

- Low-density parity-check (LDPC) FEC:
  Higher rate and Lower power than Viterbi design
DS and OFDM UWB papers

- OFDM can achieve higher data rate in the system performance requirements.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Data rate</td>
<td>61K~250Mb/ s</td>
<td>750M~1.5Gb/ s</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>125MHz~4GHz</td>
<td>1.25GHz</td>
</tr>
</tbody>
</table>
LDPC: Next-generation FEC
- 100Mb/s IEEE 802.11n WLAN
- 500Mb/s wireless FEC design [6]
480Mb/s LDPC-COFDM

✓ LDPC: High-throughput and area-saving

![Graph showing LDPC and Radix-2^n Viterbi performance comparison with 1M gate count indicated.](image-url)
### Data rate parameter

<table>
<thead>
<tr>
<th>Data rate (Mb/s)</th>
<th>Signal bandwidth</th>
<th>FEC coding rate</th>
<th>Spreading gain</th>
<th>Range (AWGN)</th>
</tr>
</thead>
<tbody>
<tr>
<td>120</td>
<td>3/4</td>
<td>4</td>
<td>13.6m</td>
<td></td>
</tr>
<tr>
<td>240</td>
<td>528MHz</td>
<td>3/4</td>
<td>2</td>
<td>11.2m</td>
</tr>
<tr>
<td>480</td>
<td></td>
<td>3/4</td>
<td>1</td>
<td>7.5m</td>
</tr>
</tbody>
</table>
System Block Diagram

From MAC Data → Scrambler → Conv. encoder → QPSK Spreading → IFFT

Channel model RF effects → Multipath channel

Timing offset → AWGN

AGC → Sync. → FFT

To MAC Data → De-Scrambler → LDPC decoder → De-QPSK De-Spreading

Viterbi decoder → Channel equalizer
480Mb/s LDPC-COFDM

✅ ADC/ DAC Wordlength Decision

Simulation environment: 480Mb/s in AWGN channel

<table>
<thead>
<tr>
<th>Wordlength</th>
<th>SNR loss for 8% PER (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>2.2</td>
</tr>
<tr>
<td>5</td>
<td>0.6</td>
</tr>
<tr>
<td>6</td>
<td>0.1</td>
</tr>
</tbody>
</table>
Fixed-point PER in AWGN channel

Transmission distance for 8% PER

<table>
<thead>
<tr>
<th>Data rate (Mb/s)</th>
<th>System requirement [1] (meters)</th>
<th>Proposed design (meters)</th>
</tr>
</thead>
<tbody>
<tr>
<td>120</td>
<td>10</td>
<td>13.6</td>
</tr>
<tr>
<td>240</td>
<td>4</td>
<td>11.2</td>
</tr>
<tr>
<td>480</td>
<td>2</td>
<td>7.5</td>
</tr>
</tbody>
</table>

Channel environment: AWGN, frequency offset: 40ppm, clock offset: 40ppm, RF filtering, phase noise
Fixed-point PER in Multipath Channel

Channel environment: AWGN, Multipath RMS delay spread: 5ns, frequency offset: 40ppm, clock offset: 40ppm, RF filtering, phase noise

<table>
<thead>
<tr>
<th>Data rate (Mb/s)</th>
<th>System requirement (meters)</th>
<th>Proposed design (meters)</th>
</tr>
</thead>
<tbody>
<tr>
<td>480</td>
<td>2</td>
<td>4</td>
</tr>
</tbody>
</table>

Transmission distance for 8% PER
480Mb/s LDPC-COFDM

System Architecture

- Scrambler and LDPC encoder
- Preamble inserter
- Clock Controlling
- QPSK and Spreading
- Shared FFT/IFFT
- Equalizer
- AGC and Sync.
- LDPC decoder and De-Scrambler
- De-Spreading and De-QPSK
- S/P
- P/S
- 5-b I/Q DAC
- 5-b I/Q ADC
- 7-b DAC
- Data From MAC
- Data To MAC
- RF

National Chiao Tung University
480Mb/s LDPC-COFDM

✅ Chip Summary

<table>
<thead>
<tr>
<th>Technology</th>
<th>UMC 0.18μm CMOS 1.8V core, 3.3V I/O</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die Size</td>
<td>6.5mm × 6.5mm</td>
</tr>
<tr>
<td>Package</td>
<td>208-pin CQFP</td>
</tr>
<tr>
<td>Transistor Count</td>
<td>4.26M</td>
</tr>
<tr>
<td>Max. Data Rate</td>
<td>480Mb/s</td>
</tr>
<tr>
<td>Max. Working Freq.</td>
<td>264 MHz</td>
</tr>
<tr>
<td>Core power @ 480Mb/s (TX/RX)</td>
<td>523mW/575mW</td>
</tr>
</tbody>
</table>
MB-OFDM techniques

- 480Mb/s OFDM and Viterbi design
- RF effect compensation (I/Q Mismatch…)
- Dynamic sampling scheme with ADDLL: ADC can be lower rate and lower power
- Integration interface to RF and MAC
MB-OFDM UWB Baseband Architecture

- **RF**
- **ADC**
- **DAC**
- **Viterbi-OFDM Transceiver**
- **MB Detector**
- **I/Q Mismatch Compensation**
- **Dynamic Sampling Tuner (ADDLL)**
- **BB/MAC Interface**
- **MAC**

Clocks:
- 2X clock (1GHz)
- 1X clock (528MHz)
System Performance (Implementation Loss)

Implementation Loss for 8% PER

<table>
<thead>
<tr>
<th>Data rate</th>
<th>Proposed</th>
<th>Standard requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>110Mb/s</td>
<td>1.5dB</td>
<td>2.9dB</td>
</tr>
<tr>
<td>200Mb/s</td>
<td>1.3dB</td>
<td>2.9dB</td>
</tr>
<tr>
<td>480Mb/s</td>
<td>1.7dB</td>
<td>3.4dB</td>
</tr>
</tbody>
</table>

Simulation condition: AWGN channel, 40ppm CFO, 40ppm SCO, and RF filters
System Performance (Transmission Distance)

Transmission distance for 8% PER

<table>
<thead>
<tr>
<th>Data rate</th>
<th>Proposed</th>
<th>Standard requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>110Mb/s</td>
<td>16.3 meters</td>
<td>10 meters</td>
</tr>
<tr>
<td>200Mb/s</td>
<td>11.6 meters</td>
<td>4 meters</td>
</tr>
<tr>
<td>480Mb/s</td>
<td>7.5 meters</td>
<td>2 meters</td>
</tr>
</tbody>
</table>

Simulation condition: AWGN channel, 40ppm CFO, 40ppm SCO, and RF filters
## Test-chip Summary

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>0.13μm CMOS 1P8M</td>
</tr>
<tr>
<td>MB-OFDM core size</td>
<td>4.0mmx4.0mm</td>
</tr>
<tr>
<td>MB-OFDM bandwidth</td>
<td>Max. 571MHz</td>
</tr>
<tr>
<td>Viterbi core size</td>
<td>2.8mmx2.8mm</td>
</tr>
<tr>
<td>Viterbi data rate</td>
<td>Max. 667Mb/s</td>
</tr>
<tr>
<td>ADDLL/PLL core size</td>
<td>1.4mmx1.4mm</td>
</tr>
<tr>
<td>ADDLL/PLL output clock rate</td>
<td>528MHz, 8 phases</td>
</tr>
</tbody>
</table>
MB-OFDM Core Power: 35.68mW (without Viterbi decoder)
I/Q Mismatch

✓ I/Q mismatch (IQM) problem: Arises in the chains of RF circuit
  - Erroneous phase difference in mixer
  - Erroneous gain in the mixer and the series of filters

✓ Equivalent signal model:
✓ CFO only
- The signal will rotate about the origin in a circle

✓ CFO and IQM
- The signal will rate about the origin in a ellipse shape
✓ **Overcome I/QM for UWB:**
  - Gain error: 3dB
  - Phase error: 10 degree
  - CFO: 400kHz

✓ **Hardware design feature**
  - Parameter tracking in pilots
  - Low processing rate to reduce the redundant power consumption

✓ **Unique Design**
  - The *pilot-tracking-based* design has a *faster convergent time* compared with the existed designs which used preamble.
  - The data distortion can be compensated in digital domain.
I/Q Mismatch

✓ Design Performance (Improvement)

PER with/without IQM compensation

- Without IQM
- With Compensation
  - Gain 3dB, Phase 10deg
- Without Compensation
  - Gain 3dB, Phase 10deg
- Design Target

Simulation condition: data rate: 480Mb/s and RF filters

| PER Improve. | 2.6 dB |
| Design Loss | < 0.3 dB |
Dynamic sampling advantages: low complexity for timing recovery

<table>
<thead>
<tr>
<th>Timing Recovery Algorithm</th>
<th>Realizable</th>
<th>Sampling Baud Rate</th>
<th>Advantage</th>
<th>Disadvantage</th>
</tr>
</thead>
<tbody>
<tr>
<td>The Proposed</td>
<td>Yes</td>
<td>1x</td>
<td>Low Sample Rate &amp; Self noise insensitive</td>
<td>AWGN sensitive</td>
</tr>
<tr>
<td>Fully ML-Based [7]</td>
<td>No</td>
<td>Infinite</td>
<td>Optimum</td>
<td>Non-realizable</td>
</tr>
<tr>
<td>Early-Late [8]</td>
<td>Yes</td>
<td>2x</td>
<td>AWGN insensitive</td>
<td>ISI sensitive</td>
</tr>
<tr>
<td>Zero-Crossing [9]</td>
<td>Yes</td>
<td>2x</td>
<td>AWGN insensitive</td>
<td>ISI sensitive</td>
</tr>
<tr>
<td>Mueller&amp; Muller [10]</td>
<td>Yes</td>
<td>1x</td>
<td>Low Sample Rate &amp; Self noise insensitive</td>
<td>AWGN sensitive CFO sensitive</td>
</tr>
</tbody>
</table>
Dynamic Sampling

✓ Dynamic sampling features
  - Reduced ADC operation power (2x->1x)
  - CFO and ISI insensitive
  - Optimum sampling position

✓ Hardware design owns following features
  - Robust circuit implementation
  - Baud rate clock processing

✓ Unique design
  - The design uses the vector-oriented decision to keep the accurate sampling phase position
Dynamic Sampling

✓ Timing Error Detector (TED) is the heart of the control loop

\[ h(t) \]

\[ C_k \rightarrow \text{Equivalent Channel} \]

\[ kT + \hat{\tau}_k \]

\[ y(kT + \hat{\tau}_k) \rightarrow \text{Decision} \]

\[ \hat{C}_k \]

\[ e(k) \rightarrow \text{TED} \]

\[ \text{Clock Source} \]

\[ \text{BPSK Data Stream} \]

\[ \text{ADPLL} \]

\[ \text{8 phase-ADPLL} \]

\[ \text{select one} \]
Dynamic Sampling

✓ Design Performance (Improvement)

PER v.s. Different Phases

- Phase 2
- Phase 8
- Dynamic Samp.
- Design Target

Simulation condition: data rate: 480Mb/s and RF filters

PER Improve. 3.1 dB
Design Loss < 0.4 dB

SNR[dB] 8 9 10 11 12 13 14 15 16

PER 10^{-2} 10^{-1} 10^{0}
ADDLL/ AD PLL Feature

- 528MHz 8-phase multi-phase clock generation.
- It is insensitive to duty-cycle of reference clock and can overcome the false-locked problem as in traditional designs.
- It can provide glitch-free multi-phase selection.
- It can be applied for dynamic sampling in A/D Converter.
- All-digital cell-based design, best portability for different processes.
- Cell-based design can reduce the design time, hence it can reduce the system turn around time.
✓ UWB Clock Generator Architecture
✓ Multi-Phase Clock Selection

1. rotate_down=1 => phase[n] to phase[n-1]
2. rotate_up=1 => phase[n] to phase[n+1]
3. To avoid glitch occurs, the phase[n] to phase[n+1] is completed by 8 times of phase[n] to phase[n-1] operation.
UWB Clock Generator Test Chip

<table>
<thead>
<tr>
<th>Process</th>
<th>UMC 0.13um 1P8M</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate Count</td>
<td>ADPLL: 5,336</td>
</tr>
<tr>
<td></td>
<td>ADMCG: 5,049</td>
</tr>
<tr>
<td></td>
<td>Multi-Phase Selector: 184</td>
</tr>
<tr>
<td>Core Size</td>
<td>ADPLL: 400um x 400um</td>
</tr>
<tr>
<td></td>
<td>ADMCG: 380um x 400um</td>
</tr>
<tr>
<td>Lock range</td>
<td>ADPLL: 200MHz - 500MHz</td>
</tr>
<tr>
<td></td>
<td>ADMCG: 528MHz</td>
</tr>
<tr>
<td>Lock time</td>
<td>ADPLL: &lt; 2us</td>
</tr>
<tr>
<td></td>
<td>ADMCG &lt; 0.3us</td>
</tr>
<tr>
<td>Avg. Power</td>
<td>ADPLL: 3.34mW(@528MHz)</td>
</tr>
<tr>
<td></td>
<td>ADMCG: 10.9mW(@528MHz)</td>
</tr>
</tbody>
</table>
Conventional FFT/IFFT

16-point Radix-4 Multipath Delay Commutator (R4MDC) [6]

<table>
<thead>
<tr>
<th>N-point FFT</th>
<th>R4MDC</th>
<th>Radix-$2^2$ FFT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory size</td>
<td>$5N/2-4$</td>
<td>$N$</td>
</tr>
<tr>
<td>No. of Complex Multiplier</td>
<td>$3(\log_4 N-1)$</td>
<td>$\log_4 N-1$</td>
</tr>
<tr>
<td>Throughput</td>
<td>$4 \times$ Clock rate</td>
<td>Clock rate</td>
</tr>
</tbody>
</table>
The Proposed FFT/IFFT

Mixed-radix Parallel FFT Architecture

Radix-2
- MEM: 64
- BUx4

Radix-8
- BU
- BU
- BU

Inputs (4,6) → (4,10) → Outputs (4,6)

Constants

Modular Complex Multiplier
FFT/IFFT Hardware Complexity

- **Memory size**
  - SRMDC [2]: 318
  - Proposed: 124

- **Equivalent Complex Multiplier**
  - SRMDC [2]: 10
  - Proposed: 4.72
High speed Viterbi decoder for MB-OFDM system

- Constraint length $K=7$
- Base code rate $R=1/3$
- Puncture code rate: $11/32$, $1/2$, $5/8$, $3/4$
- Maximum data rate: $480\text{Mb/s}$ ($R=3/4$)

Implementation

- Radix-16 ACS unit
- Register-exchange based SMU
- 3-bit soft input
- 9-bit path metric
Viterbi Decoder

✔ Chip summary

<table>
<thead>
<tr>
<th>Feature</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.13um</td>
</tr>
<tr>
<td>Chip size</td>
<td>7.6mm²</td>
</tr>
<tr>
<td>Max. data rate</td>
<td>667Mb/s @ 1.02V</td>
</tr>
<tr>
<td>Power consumption</td>
<td>400mW @ 1.2V</td>
</tr>
</tbody>
</table>
High speed (1200,720) LDPC decoder
- Decoding speed reaches Gb/s at 8 decoding iterations
- Increase the chip density to above 70%

Time-multiplexed decoder design
- Map a certain number of nodes to a single operation unit.
- A trade off between complexity and decoding speed.
✓ Message-passing algorithm

- Check-node update (implemented by min-sum algorithm):

$$\Lambda_{cm} \approx \prod_{m' \in M(c) \cap m} \text{sign}(\lambda_{m'c}) \times \min_{m' \in M(c) \cap m} (|\lambda_{m'c}|)$$

- Message-node update:

$$\lambda_{mc}(u_m) = L(u_m) + \sum_{c' \in C(m) \setminus c} \Lambda_{c'm}(u_m)$$
Architecture

- Use 2 memory banks to decode 2 codewords at the same time.
Memory allocations

- \( CU_i^j \):
  - The check-node set of block \( i \) that operated in the \( j \)th CU update cycle.

- Store values in a interleaved manner.

- Partition the memory bank into 4 parts based on the parity-check matrix \( H \).

Interleaved Storage
Modification of memory allocations

Original

Modified

Each register in section B (or C) is connected to multiple MUs and CUs, which make large congestion.

Only registers in A&C connect to MUs (or CUs), and only those in B, C, and D connect to CUs (or MUs).
5Gb/s LDPC Decoder

✅ Chip Summary

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.18um 1P6M</td>
</tr>
<tr>
<td>Chip size</td>
<td>25 mm²</td>
</tr>
<tr>
<td>Gate count</td>
<td>1.15M</td>
</tr>
<tr>
<td>Max. data rate</td>
<td>3.33Gb/s @1.62V</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>644mW @1.8V</td>
</tr>
</tbody>
</table>
5Gb/s LDPC Decoder

✓ Chip Summary

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.13um 1P8M</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip size</td>
<td>13.5 mm²</td>
</tr>
<tr>
<td>Gate count</td>
<td>1.15M</td>
</tr>
<tr>
<td>Max. data rate</td>
<td>5.8Gb/s @1.02V</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>268mW @1.2V</td>
</tr>
</tbody>
</table>
Conclusion-I

✓ Trade-off between system performance and power dissipation for Wireless communications SoC;

✓ More Hardware-Oriented/Software-Oriented PHY/Protocol solutions;

✓ Joint-effort of Multi-Disciplinary research teams with unique features and capabilities.
✓ UWB standard: Leads the market of future WPAN and portable media products;

✓ UWB chipsets: High performance, low power, and short time-to-market;


